

# RELIABILITY TESTING FOR MICROVIAS IN PRINTED WIRE BOARDS

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## ABSTRACT

Traditional single level microvia structures are generally considered the most robust type of interconnection within a printed wire board (PWB) substrate. The rapid implementation of HDI technology now commonly requires between 2, 3 or 4 levels of microvias sequentially processed into the product. Recent OEM funded reliability testing has confirmed that by increasing the levels (stack height) these structures are proving less reliable, when compared to their single or double level counterparts. Recently false positive results have been recorded on products tested with traditional thermal shock testing methodology (cycling between -40°C and 125°C, or 145°C). A number of companies are incurring product failures resulting in increased costs associated with replacing the circuit boards, components and added labour.

## INTRODUCTION

This paper addresses new developments for establishing microvia interconnect reliability, using elevated thermal cycle testing of representative coupons. Improvements in the accuracy of testing are achieved by means of increased sensitivity in the test vehicle (coupon) designs, improved test methods, and more accurate failure analysis. Test methodologies for microvia structures built with FR4 used elevated testing temperatures of 190°C, slightly above the glass transition temperature (T<sub>g</sub>) and higher temperatures when testing polyimide dielectric materials (230°C). The reliability implications of various microvia configurations including stacked, filled, and microvias stacked onto internal buried vias will be reviewed. Concerns and considerations for microsection preparation, microvia defect location and the anatomy of a robust microvia are presented. Six microvia failure modes are described.

The implementation of high density interconnect (HDI) structures, containing multi-level micro via constructions has created a growing number of technical challenges. Those challenges include a balance of electrical properties, quality conformance and product performance. Virtually all segments of the electronics industry are now confronted with the reality that conventional assessment techniques and measurement criteria have limited ability to confirm that product will be robust through assembly and in their end use environment.

European legislation has meant that lead-free solders now dominate mainstream electronic manufacturing. These lead-free replacement solders are typically high tin alloys with significantly higher melting points as compared to conventional tin-lead solders. Dielectric material technology has been developed to resist degradation at the higher process temperatures required by the new solder alloys. The products exposure to multiple assembly and potential rework cycles at these higher temperatures, places both the copper interconnections and base materials at risk. Before undertaking any reliability testing the coupon should be designed to consider both aspects of product performance.

The introduction of multi-level microvia structures has happened in parallel with the increases in assembly temperatures, the combined influence has resulted in increased levels of strain applied to the interconnect structures and surrounding materials. The elevated assembly (and rework) temperatures have reduced the reliability of interconnect structures and increased the risk of microvia and material failures. This paper addresses how microvias may fail in response to the thermal excursion associated with assembly and the end use environment.

The logic of different elevated temperature testing on FR4 and polyimide base materials are reviewed. Also addressed will be micro-sectioning techniques to improve the acuity of microscopic analysis. The failure modes addressed include separation between the base of the microvia and the target pad, barrel cracks, corner cracks, circumferential cracks around the top of the microvia and the capture pad and microvia mis-registration.

**TEST METHODOLOGY** – Microvia testing is performed with Interconnect Stress Testing (IST) using a modified methodology documented in the IPC Test Methods Manual TM650, Method 2.6.26, titled DC Current Induced Thermal Cycle Test. Microvia reliability testing for FR4 modifies the documented test methods stated temperature from the default of 150°C, up to 190°C, this temperature level is required to enunciate microvia failures without producing artifacts or artificial failure modes. Testing at the lower default temperature of 150°C can not effectively or accurately find failures within 1000 cycles (4 days of testing), on coupons associated with printed circuit boards that had a 30% fall-out rate in surface mount assembly (Andrews, Parry, Reid 2005).

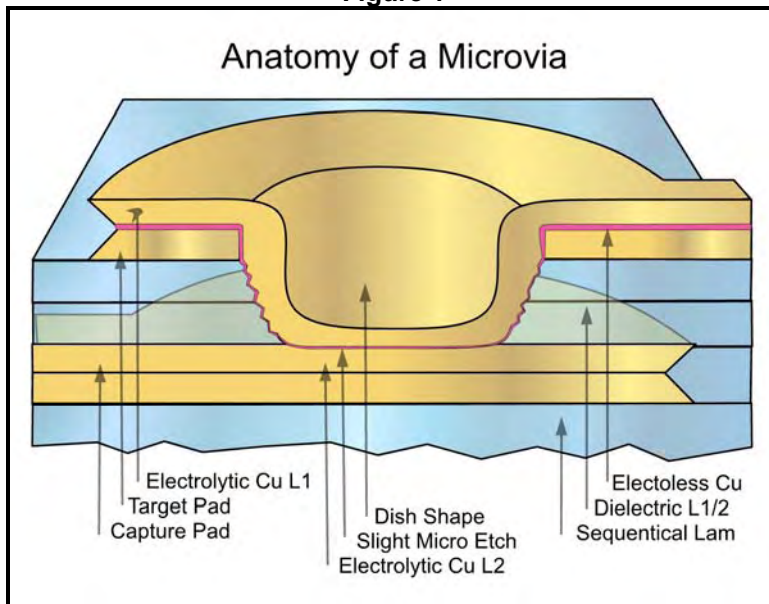
Two of the unique advantages of using this technology are the ability to complete high speed continuous monitoring of all circuits throughout each thermal cycle and that stress testing stops individually on each coupon at a 10% increase in resistance, for each specified test circuit. The measured increase in resistance is a direct reflection of the level of damage accumulated within the specific test circuit, at a 10% change cracks or separations are established, but have not fully progressed to a point of an open (intermittent high resistance). This capability (to halt testing and damage accumulation) allows failure analysis to be processed before the failure sight is compromised, as it would be if testing was continued beyond a low level of resistance change.

Reliability testing has confirmed microvias are usually the most robust interconnect structure in a PWB, when compared to the PTH, buried vias and blind vias. Testing has also confirmed that unreliable microvia can survive thousand of cycles when thermally cycled to temperatures of 150°C, or below. Any test temperature below the Tg of the material appears limited in the ability to discern good from bad microvias. Testing has also confirmed that well fabricated (robust) microvias do not fail for thousands of cycles, when tested to the temperature of 190°C.

**MICROVIA OVERVIEW** - For the purposes of this paper a microvia is defined as a single or sequentially laser ablated blind interconnection, with a diameter of 0.15 mm (.006”) or less. Microvias are most commonly ablated through thin dielectric materials (FR4, resin coated copper or polyimide) to enable a conductive interconnection to be formed between adjacent layers (L1 to L2, L10 to L9, Etc.), although ablation through two (L1 to L3) and three layer (L1 to L4) interconnections are now becoming more common. Controlled depth drilling and plasma etching are alternative techniques, but are less commonly used in volume production of HDI products.

The anatomy of a well produced microvia is processed with a dish shaped profile (see figure 1), rather than a straight or angle sidewall. Processing should achieve an even distribution of electroless copper and electrolytic copper, from the surface foil capture pad down to the target pad. The side wall of the microvia should be relatively smooth, with minimal glass fibers protruding into the microvia, which has proven to inhibit the ability of chemistries to penetrate down onto the target pad.

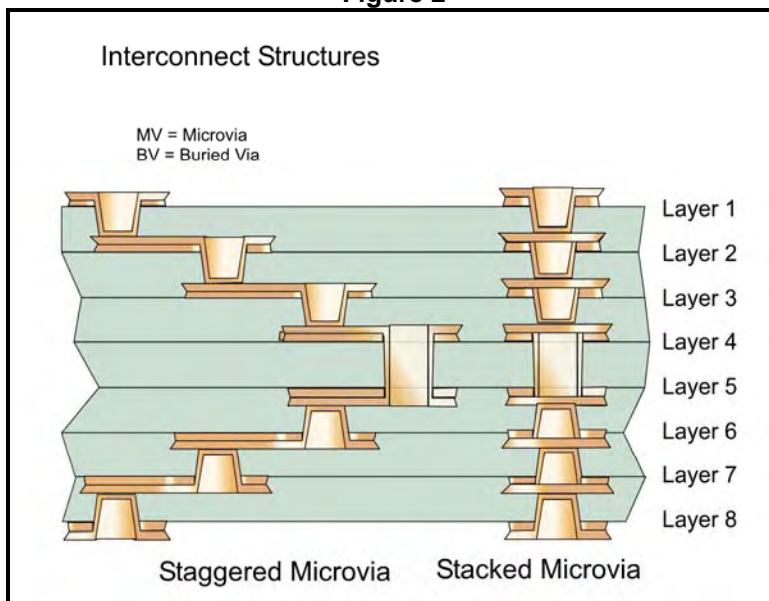
Figure 1



Note: The terms capture pad and target pad are commonly interchanged to describe the pad at the base of the microvia. The IPC T50 - Terms and Definitions document states the following; "The first conductive layer penetrated in microvia fabrication is ablated through the capture pad and the conductive layer where the microvia terminates is the target pad".

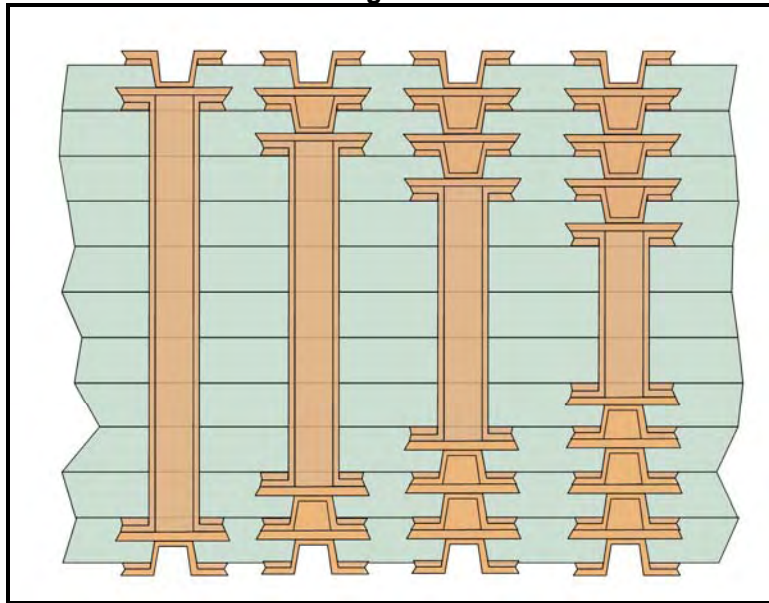
Microvia produced over the past 5 to 10 years are commonly created between two adjacent layers, but the advent of products requiring HDI technology, especially hand-held computers necessitate multi-level microvias that traverse sequential layers. Each level of microvias may be staggered in an offset arrangement or stacked on top of each other in the same x/y location (See Figure 2).

Figure 2



Stacked microvia require duplicating and/or additional process steps in fabrication, including the filling of the microvia which establishes an ability to sequentially ablate additional vias into a structure containing 2, 3 or 4 microvias stacked on both sides of the substrate (See Figure 3).

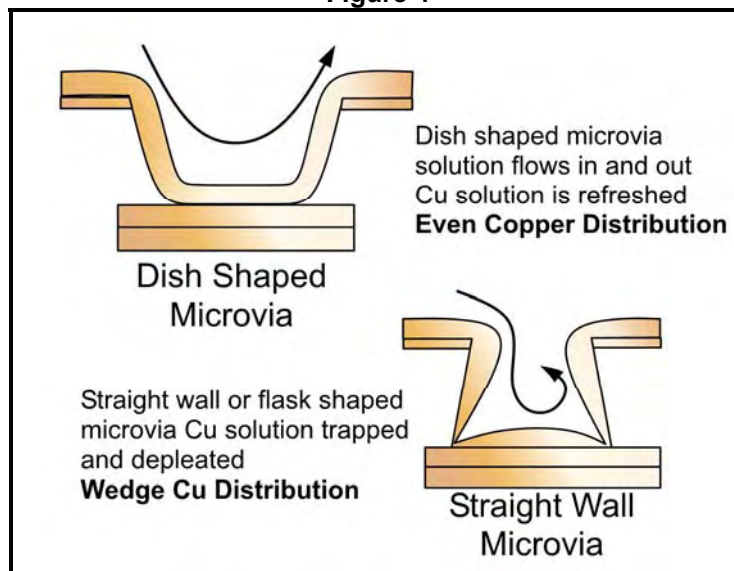
Figure 3



Via filling can be categorized by the types of fill. a) Microvia filled with epoxy resin (b-stage) during a sequential lamination process step, b) A third party non-conductive or conductive fill applied as a separate processing step, c) Plated closed with electroplated copper, d) Screen printed closed with a copper paste. Microvia filled with a conductive fill or non-conductive fill other than copper require, a conductive layer (copper cap) be processed onto the top of the microvia fill material.

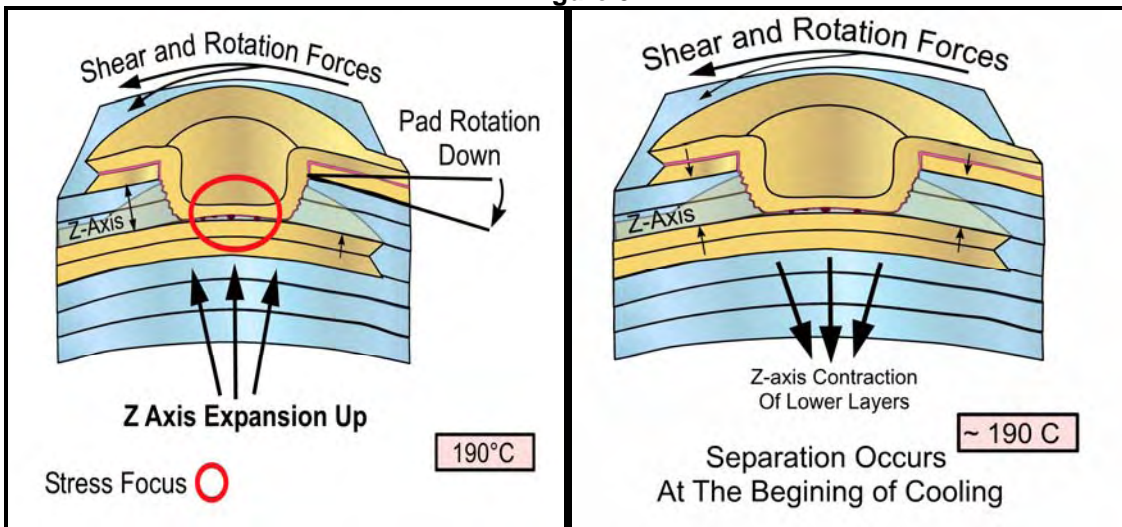
The critical processing steps involved in producing a reliable conductive structure capable of carrying an electrical current between two or more layers includes; laser ablation, chemical cleaning, “desmearing” (chemical removal of excess resin), micro-etching, electroless copper or direct metallization, electrolytic copper plating and possibly hole filling. The small geometries of the microvia features create a number of complex manufacturing challenges, requiring excellent process controls in both equipment and in the processing lines that most affect the capability to produce consistent conditions (laser ablation, metallization line and electroplating line). The fundamental considerations are relative to the surface tension and that fluid viscosity limits the numerous process chemistries ability to remove spent solutions and replace it with fresh chemistry (See Figure 4).

Figure 4



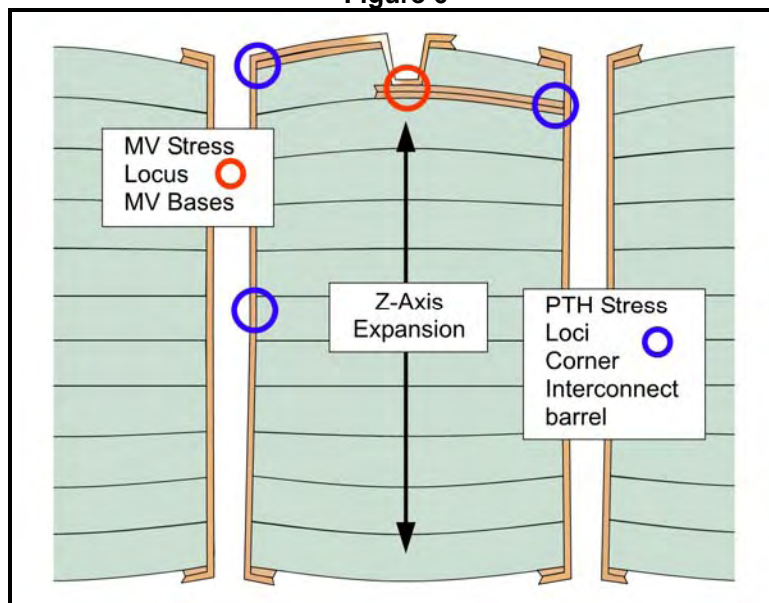
**THE PHYSICS OF MICROVIA FAILURE** - The majority of the strain exerted on a microvia is from the Z-axis expansion of the dielectric. As the dielectric is heated it expands. The coefficient of thermal expansion (CTE) is the change in thickness of the dielectric per degree centigrade. The CTE of dielectric materials used in PWB fabrication are measured in part per million per degree centigrade (ppm/C). Thermal analysis of the FR4 epoxy glass laminate show a CTE that is constant until the glass transition temperature (Tg). At the glass transition temperature the CTE increases by a factor of 8 to 10. A typical CTE of a multilayer PWB is around 30 ppm/C before Tg and then increase to 250 to 300 ppm/C after Tg. Tg is usually found to be between 150°C and 180°C. at temperatures above Tg the amount of strain exerted on the system is significantly increased (See Figure 5) .

Figure 5



Because the microvia dielectric is very thin (0.05mm/.002" to 0.15mm/.006"), the amount of strain in the microvia structure is low as compared to a PTH or other interconnect structures. Figure 6 illustrate the most common location where stain is applied to PTH and microvia structures. Considering is the PWB is correctly fabricated, the hierarchy of influence for stain distributions is as follows; PTH barrel (central zone), corner/knee, internal interconnect, followed lastly by the microvia. In the typical HDI board construction the microvias are frequently found only on the outer layers of the board, the surface layers are not inhibited and move in unison with the z axis expansion, creating a movement like a "springboard", literally moving freely without constraint

Figure 6

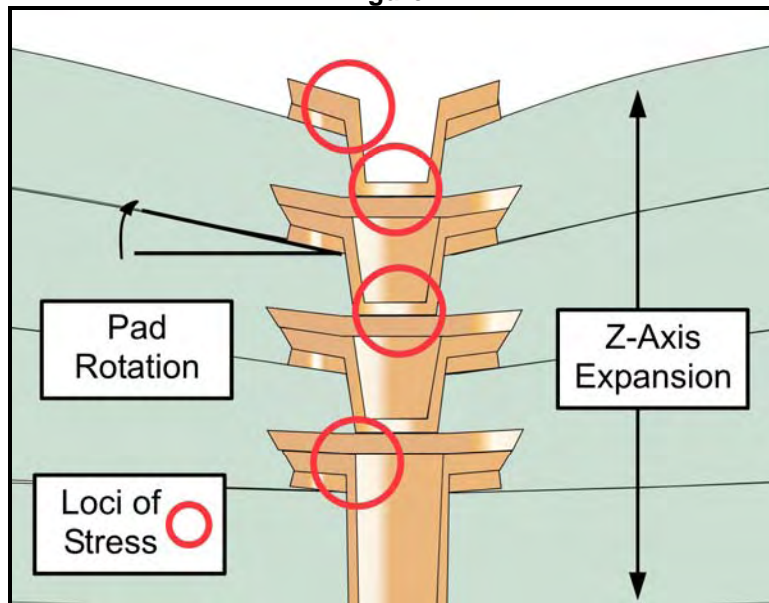




The CTE of the dielectric below the microvia is the same as the CTE of the dielectric around the microvia structure, assuming the same materials are used. Because there is a greater volume of dielectric below the microvia there is a much greater amount of expansion occurring below the microvia. The main cause of strain on the microvia during thermal excursions is from the Z-axis expansion of the dielectric between the top of the microvia (outer layer) and the capture/target pad. The amount of strain exerted in the microvia structure is in proportion to the thickness of the dielectric. The amount of stress in the system is a function of dielectric thickness, surface area, shear forces and the visco-elastic properties of the dielectric material. In this paper we will limit the discussions to stress/strain.

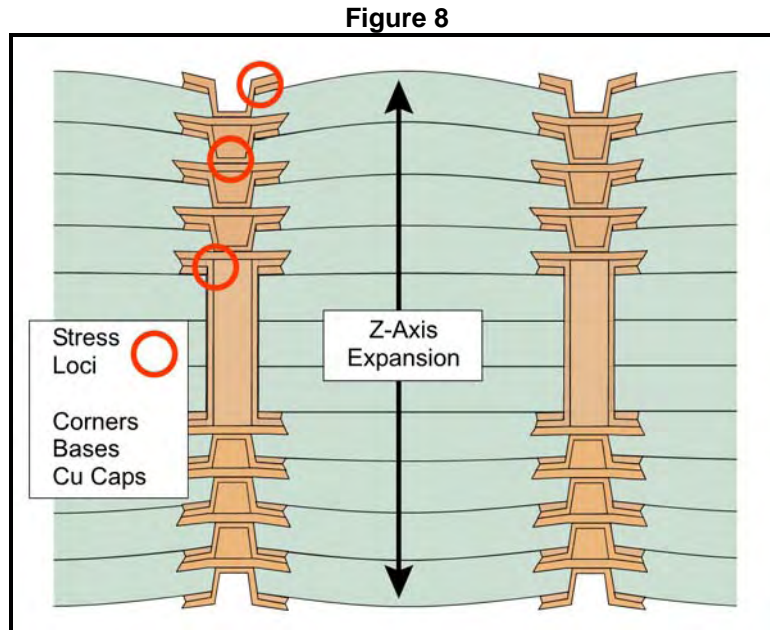
Obviously, as additional vias are added to the structure the stress levels are increased relative to the increased dielectric distance between the upper capture pad and lower target pad. The focus of the stress concentrations are now distributed over a wider range of interconnections, primarily any interface between each two levels of microvias (See figure 7).

Figure 7



The situation is further complicated by the relocation of the anchor point (locking or constraining position), moving the lowest part of the structure closer to the central plane of the board construction. Because the structure is now constrained by the minimal z axis expansion in the middle of the board, compared to the higher (unconstrained) z axis toward the surface, a stress is created throughout the structure. If stacked microvias are attached either side of a buried via, especially one that traverses the middle two layers, the structure is now totally inhibited and takes on the inherent aspects of a through hole (top to bottom) structure. This condition now introduces additional x, y stresses on the structure which effectively contains a relatively high aspect ratio (board thickness ÷ via diameter) via, compared to their drilled and plated counter-parts

Figure 8 describes the appearance of a “4 n 4” construction, where a PTH is not used in the product to create an interconnection. For this type of build the hierarchy of influence for failure are relatively equally divided across the lower attachment to the buried via, corner/knee and central zone of the via stack. The buried via is generally created on a thin dielectric material and is not usually affected by x, y axis expansion . The exception to this rule is when a plated cap is applied on either side of the buried via, the buried via can experience higher level of z axis being applied by the stacked via “pulling away” from either side (see failure modes for more details).



The hierarchy of failure would normally be applied equally on both sides of the construction, although the deciding factor would be the component placement used in the actual product. If a large device (BGA etc.) was attached on the top side, the additional detrimental influence of the CTE mis-match between the FR4 and package material would bias the hierarchy toward the device side of the substrate. The resulting loads would be a combination of thermal (x, y and z axis) and mechanical stresses applied (device moving upwards and away) to the structure.

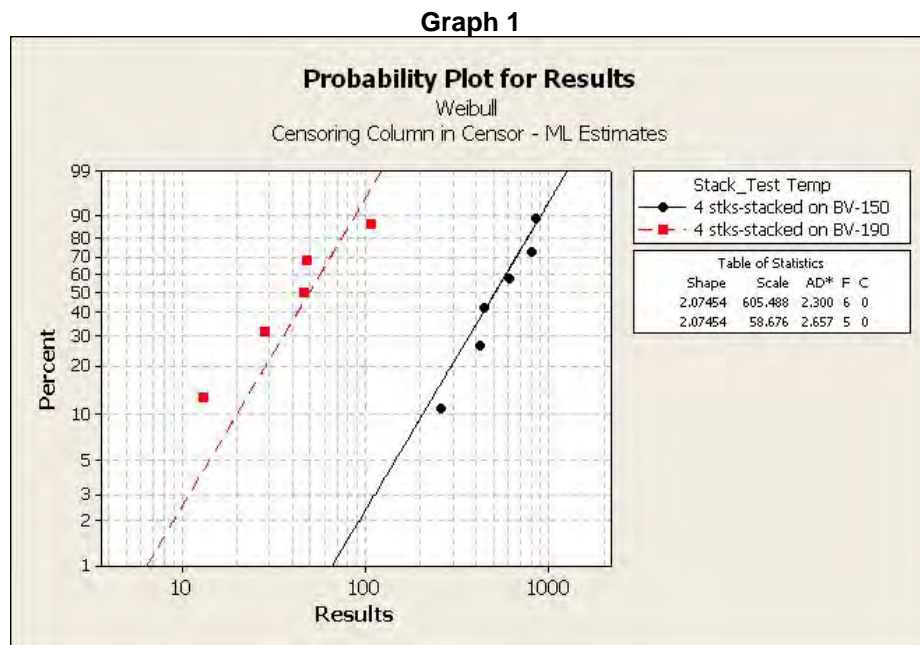
**STATISTICAL ANALYSES** – Two statistical methods are commonly used in data analysis of reliability test data. The two methods are Standard Statistical Analysis (mean, minimum, maximum, standard deviation, coefficient of deviation, Cp, CpK etc.) and Weibull Analysis (beta, eta, mean, MTBF, standard deviation etc).

**STANDARD STATISTICAL ANALYSIS** - This includes calculations of mean, standard deviation, coefficient of variation, minimum, maximum, and range. The mean is the average cycles to failure or end of test. The limitation of this method is that, by convention, coupons that are stopped at end of test are considered failures. Data that contains end of test results as failures is called right-censored data. The standard deviations reflect the variation in cycles to failure from the mean. The number calculated for testing purposes is the first sigma limit. The mean plus or minus the sigma limit would include 68.2% of the failed coupons. This is true if the distribution of cycles to failure (histogram) is a perfect “Bell Shaped” curve. The problem is that the distribution of cycles to failure is rarely truly bell shaped. Frequently there are two or more failure modes active in the coupons and the distribution curves become distorted. The minimum is the earliest failure and the maximum is the highest number of cycles a coupon achieves. The range is the difference between the minimum and the maximum. The coefficient of variation is the mean divided by the standard deviation expressed as a percentage. Coefficients of variation above 100% and below 1% are considered meaningless.

**WEIBULL ANALYSIS** – Weibull analysis is routinely used in reliability studies. Weibull statistical analysis has two distinct advantages. Weibull analysis requires that data is entered as either the number of cycles to failure or the number of cycles achieved when the test was suspended. Suspended test data is given extra weight. Weibull analysis also allows the shape of the distribution to be varied in accordance to the actual distribution. Weibull data recorded includes beta and eta, mean, standard deviation, mean cycles to failure. Beta is the shape parameter, a beta of 3.6 is a bell curve, beta of 1 is an exponential distribution (long and flat), and a beta of 5 may be described as a “peaked normal” distribution. Eta is defined as the scale parameter or characteristic life. The characteristic life is the point where 63.2 percent of the coupons have failed. Weibull also allows the user to graph a number of plotting options. The two basic plots include Weibull Plot and probability density function (PDF) graphs. In the Weibull graph steepness of the graph indicates the spread of data. The steeper the slope more tightly the data is correlated. The position of the line in the X-axis indicates the range of the data. A PDF graph looks a lot like a histogram but it is in reality the distribution of the probability of when coupons fail and has the advantage of allowing an easily understood visualization of coupon failures.

This paper will describe the results of reliability testing using Weibull probability plots comparing differences in test conditions, levels of vias in the structure, stacked vias with and without connections to a buried via and stacked versus staggered via configurations.

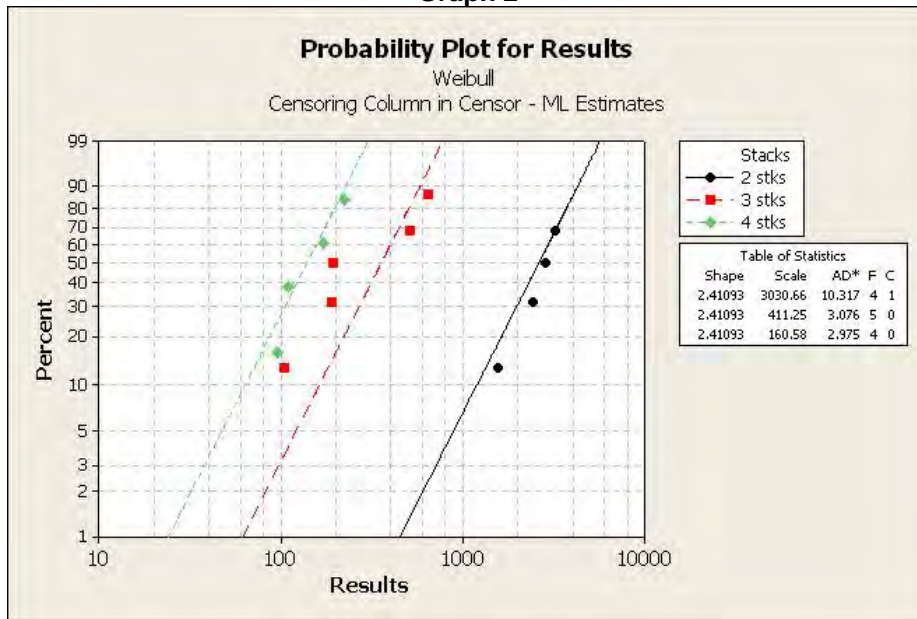
Graph 1 is critical to the importance of understanding why higher test temperatures are required to discern acceptable from questionable results from microvia testing. Identical coupons produced on the same test panel with 170°C Tg material, constructed with 4 stack microvias on either side of a buried via, were tested without assembly stresses at temperatures of 150°C and 190°C. The mean cycles to failure ranged from approximately 600 to 60 respectively, a 10X acceleration. From a test time perspective this equates from 3 days to 5 hours on IST, the equivalent cycles in the thermal shock oven would be 24 days (probably even longer because of the lower test temperature). The performance achieved in the 150°C testing would have been considered acceptable to virtually all documented customer specifications.



The shape of the lines are virtually the same, this indicates that the failure mode is expected to be the same. The results in graph 1 do not appear that unusual until the performance of the 4 stack microvias are compared to similar products (built on the same test panel) constructed with fewer levels within the stacked microvias. Graph 2 compares 2, 3 and 4 stack structures, not on a buried via, tested at 190°C. The shape of the lines again confirm similar failure modes should be expected, despite the differences in constructions.

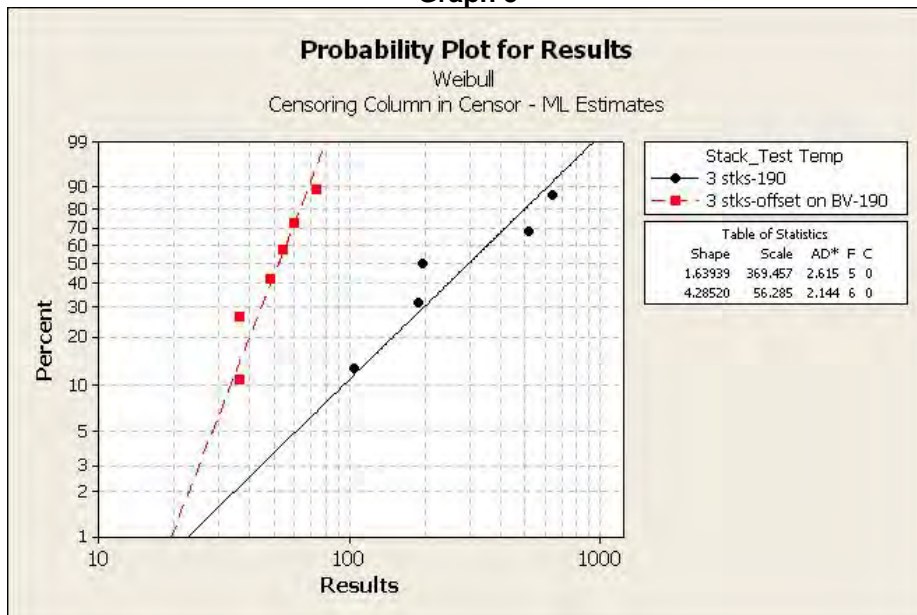


**Graph 2**



The mean cycles to failure range from approximately 3000 (2 stack), 400 (3 stack) and 160 (4 stack). It is now possible to establish a relative performance between the different structures, clearly the migration from 2 stack to 4 stack demonstrates a potential for a 20X reduction in cycles to failure. What is also important to consider is that the 2 stack construction achieved a mean of 3000 cycles when tested at 190°C, subsequent failure analysis confirmed the material was not severely degraded by the excessive cycling at relative high temperature. From a test time perspective duration ranged from 12 days, 2 days to 17 hours respectively. Thermal shock ovens would take approximately 120 days to complete 3000 cycles.

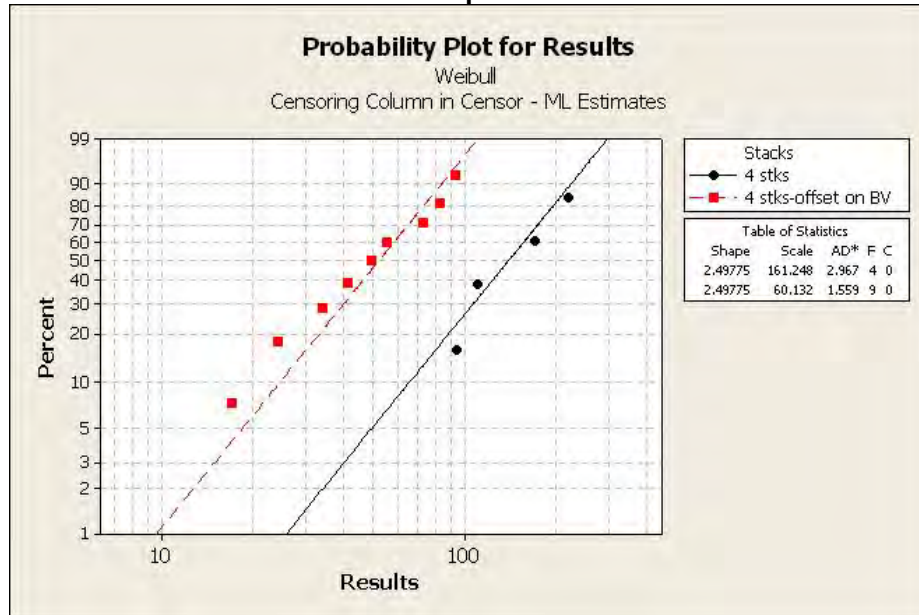
**Graph 3**



Graph 3 compares 3 stack microvias with and without attachment to a buried via. Firstly, the line shapes are different, indicating that the two configurations failed in different ways. Although the 3 stack on buried via failed relative early (mean 56 cycles), the shape of the data is consistent, meaning that predicting the performance can be completed with high confidence. The 3 stack without buried via attachment is quite scattered, indicating that more than one mechanism is responsible for the failure

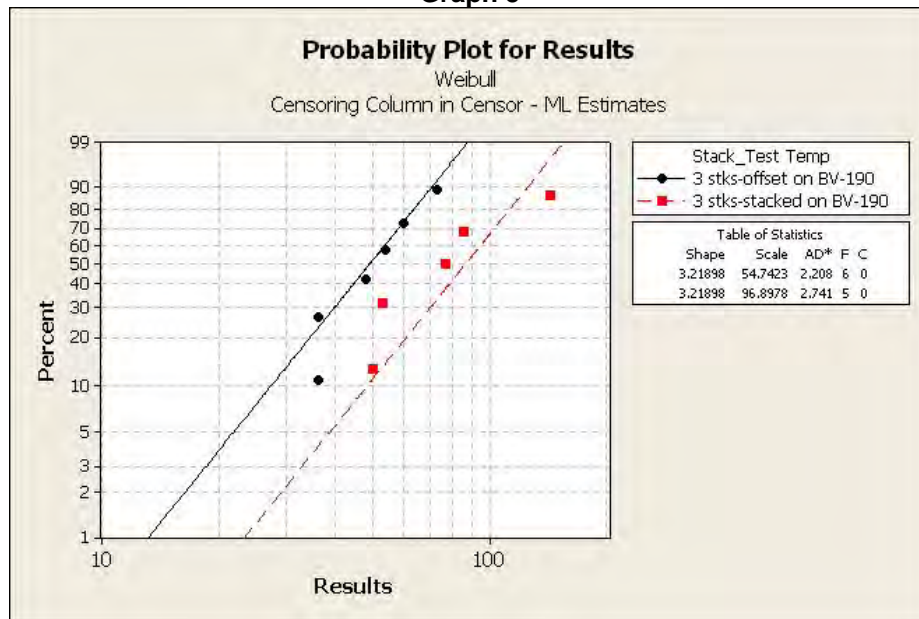
Four stack with and without attachment to a buried via are compared in graph 4. The cycles to failure are dramatically reduced, the mean without buried via attachment was approximately 160 cycles, with buried via 60 cycles. The trend is consistent to the 3 stack results confirming the attachment to the buried via is detrimental to the performance of the stack via structures. The line shapes are similar, so the expectation is that the failure is occurring in the same location within the stack structure

**Graph 4**



Graph 5 compares 3 stacked microvias attached to a buried via versus 3 staggered microvias, with the lowest microvia being attached to the buried via (see figure 2 for illustration of stacked and staggered).

**Graph 5**



Neither of the two configurations performed that well, but the stacked vias demonstrated nearly double the cycles to fail. With this type of result failure analysis would be performed to understand the reasoning for the difference in performance.

**TRADITIONAL MICROVIA FAILURE MODES** – Based on the hierarchy of influence and the mechanics of failure related to how damage accumulates, microvias can be sorted into six general failure mode categories; interface separations, barrel cracks, corner cracks, target pad cracks, mis-registration and stacked microvia specific.

**STACKED MICROVIA SPECIFIC FAILURE MODES** - When two or more microvias are stacked together additional failure modes are observed. The primary reasons are; a) the combination of increased strain levels (stress) around the multi-level vias, applied to the higher aspect ratio structures. b) Moving the “anchor point” of the target pad closer toward the central plane of the construction, or connecting to an internal feature, like a buried via. c) Changing material properties created during the first, second and third (and sometimes forth) lamination cycles, causing the originating material to undergo several exposures of curing times and temperatures, which risks the on-set of material degradation, lower flexibility and reduced ability to avoid material damage (delamination) during the assembly process. d) The complications associated to multiple passes through the metallization and electrolytic plating processes, via filling, copper planarization operations. e) Via to via registration.

**INTERFACE SEPARATIONS** – The most common failure mode for microvias is a separation between the base of the microvia and the target pad. This failure mode presents itself as a catastrophic failure that is usually observed as the structure enters into a cooling phase. The condition is created by a number of factors, but the most common root causes are; Under-ablation, where resins are not sufficiently removed due to incorrect energy levels or poor trepanning techniques, creating a non-conductive barrier between the target pad and subsequent metallization (See Photo 1).

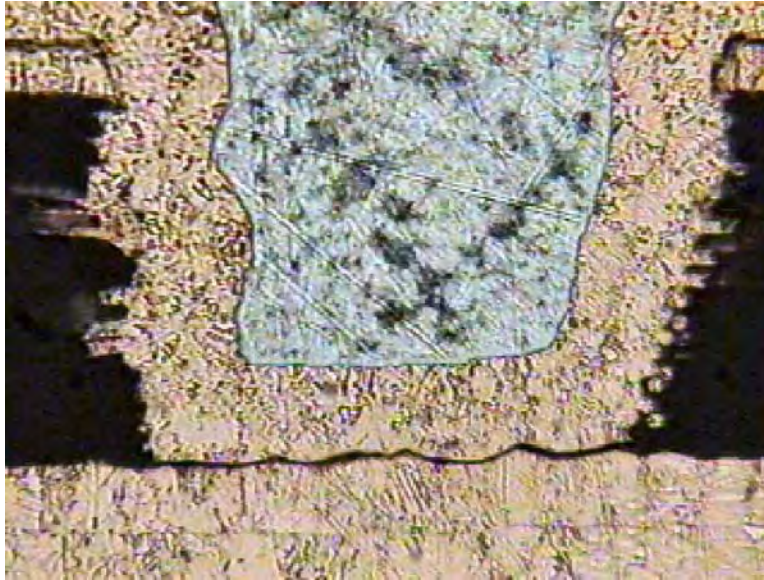
**Photo 1**



Poor/Limited micro-etching of the target pad, preventing a strong chemical bond from being established, the area below the microvia should exhibit a slight micro-etch, this confirms the target pad was chemically cleaned before the copper plating was deposited into the via.

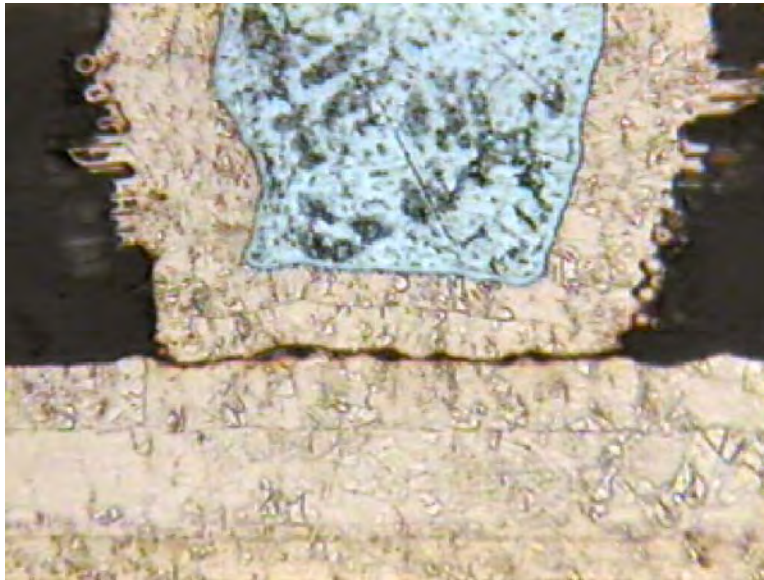


**Photo 2**



Insufficient desmear causing the by-product from the ablation process (ash) to become entrapped at the interface between different metal layers, this residue creates perforations (small spherical matter) between the metals and weakens the critical chemical bond.

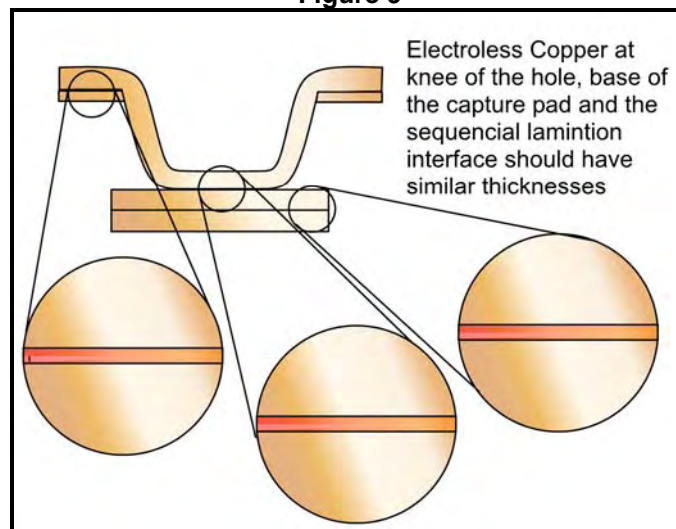
**Photo 3**



The absence of electroless copper on the target pad, which creates an electrolytic copper to copper foil interface, or electrolytic copper to electrolytic copper interface, neither creates a strong bond. The fact that no electroless copper is present on the target pad is a strong indicator that other chemistries prior to the copper plating bath also had difficulties achieving their function, resulting in insufficient surface preparation to enable a strong foundation for the base of the microvia.

Confirming the presence of evenly deposited electroless copper is an important function during failure analysis. In some PWB manufacturing facilities the electroless copper is followed with a thin electrolytic copper flash, designed to “protect” the electroless in subsequent processing. Figure 9 is designed to indicate the areas that should be visually compared for determining the consistency of the electroless deposit.

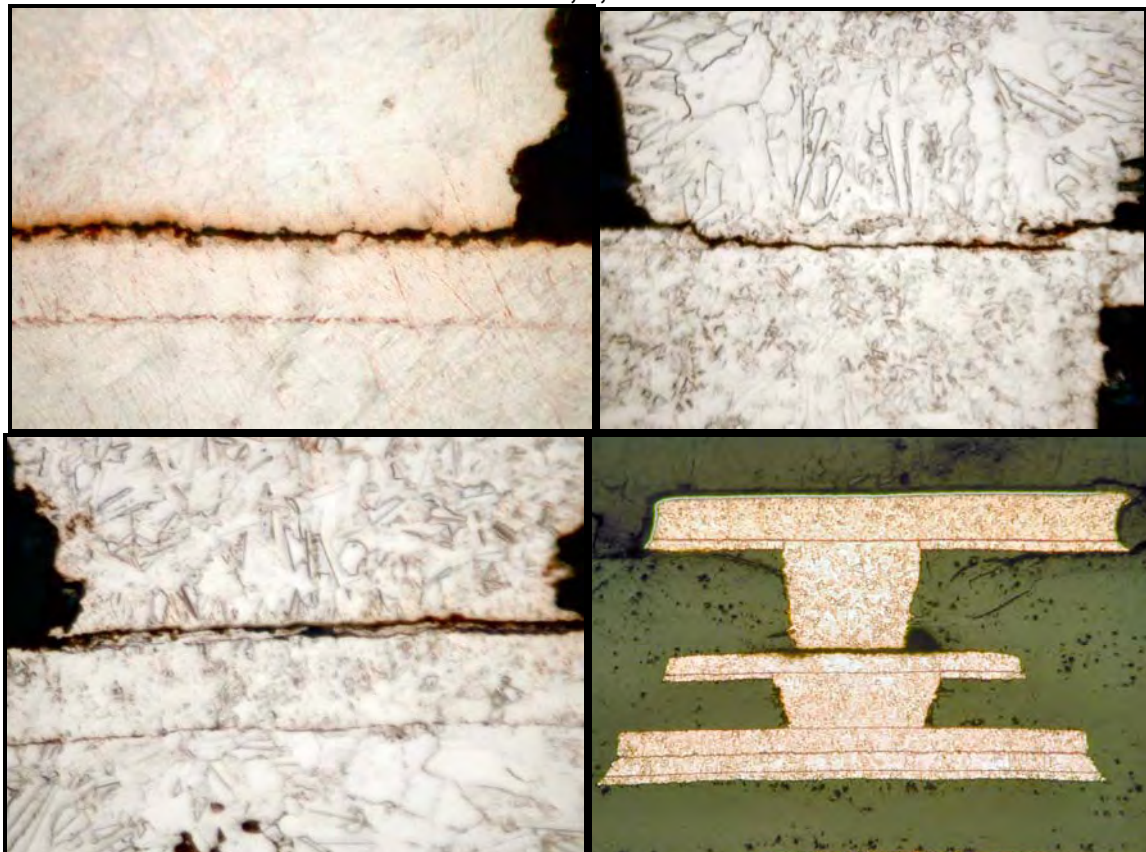
**Figure 9**



Note: If the PWB supplier is using a direct metallization (palladium, carbon, conductive polymer, etc.) plating line there will/should not be a demarcation line between the different copper deposits. This situation makes the failure analysis more complicated when attempting to determine the root cause within the manufacturing process. When completing any reliability testing on microvia structures it is important to understand the method of metallization used and convey this information to the individuals or companies responsible for completing the failure analysis.

Photo's 4 through 7 are associated to different types of interface failures, they are not intended to be inclusive, but give illustrations of the many diverse appearances that are commonly found with microvia failures.

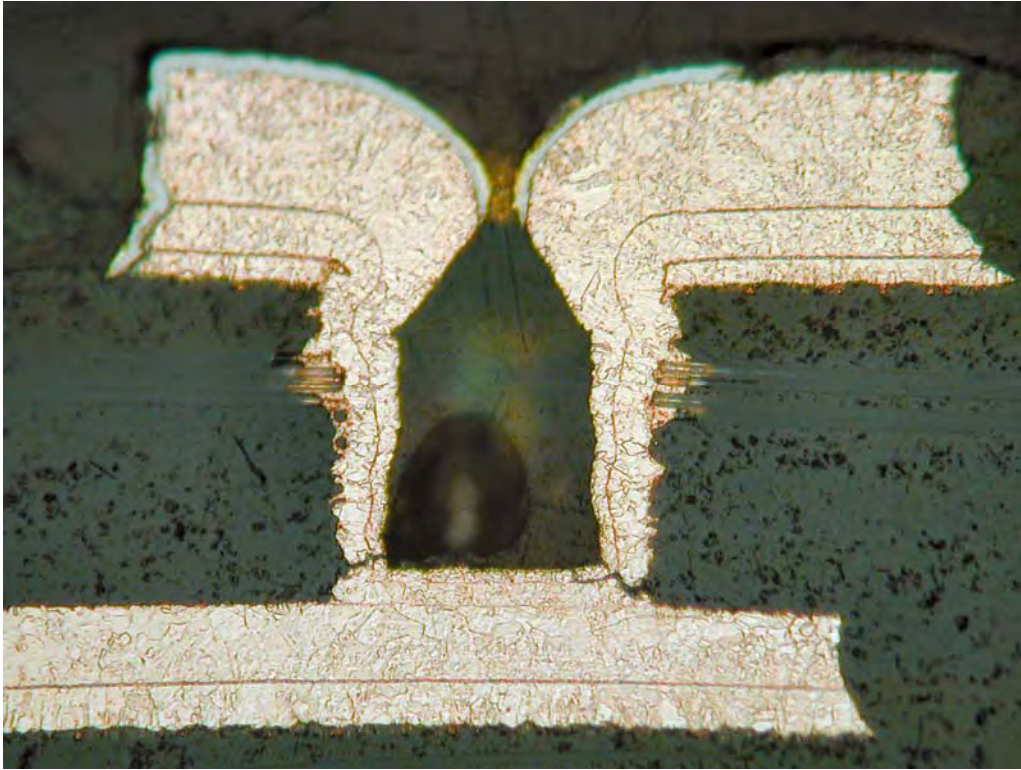
**Photo's 4, 5, 6 and 7**





**MICROVIA BARREL CRACK** – A barrel crack is associated with thin (often localized) electrolytic copper plating, usually found with a taper toward the base of the microvia. It is common to see a thick copper deposit near the surface, reducing down to very thin at the point of attachment to the target pad.

**Photo 8**



All plating irregularities/problems are principally related to a dysfunctional combination of chemistry and equipment. In many cases PWB manufacturers use different suppliers for various chemical components within the metallization line; this can create chemical incompatibilities between critical preparation steps (cleaning, desmearing, micro-etching, glass-fibre etching, conditioning, activation, etc.) The type of equipment used must be considered of primary importance to the success of achieving an overall capability and compatibility, the chemical supplier and equipment supplier should be working in concert, as a single entity to assure the ability to produce consistent and robust microvia structures. Reliability testing confirms that a crack in the barrel of a microvia is a wear out type failure mode. The via can withstand the high stress associated with assembly, without creating an intermittent connection, over time the conductive path will degrade and result in a high resistance, or open state.

**Photo's 9 and 10**



**MICROVIA KNEE/CORNER CRACK** – A crack that occurs at the junction between the microvia knee/corner and the capture pad, The cracks are often present in products that experience an overly aggressive copper removal operation (planarization), resulting in very thin pads, usually only copper foil remains, with all microvia electrolytic copper plating being removed.

When the knee/corner plating is removed it creates a “butt-joint” junction between the pad and via plating, during pad rotation this junction is compromised. The damage is initiated by high z-axis expansion of the dielectric between the capture pad and the target pad, commonly during component assembly, or more probably a local rework procedure. Considering that conventional operating temperature and the dielectric spacing between the two layers, which is commonly between 0.05mm (.002”) and 0.15 mm (.006”), it is unlikely that enough CTE can be generated to initiate damage, or propagate a crack. The concern for this failure mode would be the CTE mismatch between the PWB and the device, which would result in increased pad rotation caused by the mechanical stress “pulling” the pad off of the upper section of the microvia. An analogy to this condition would be pad-cratering, where the surface pad is literally torn away from the outer surface resin. If the junction between the microvia and surface pad are compromised this failure mode could materialize. Following crack initiation a microvia knee/corner crack is a wear out type failure.

**Photo 11**



**Photo 12**



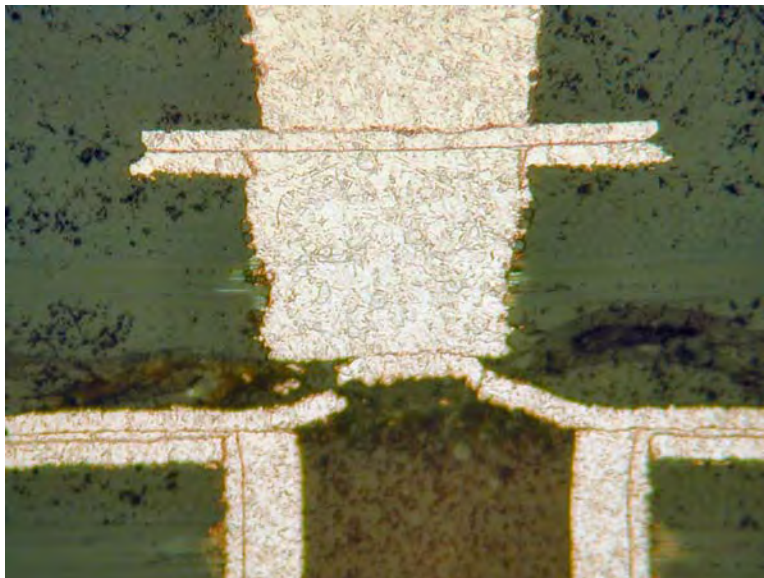


Photo's 13, 14, 15 and 16

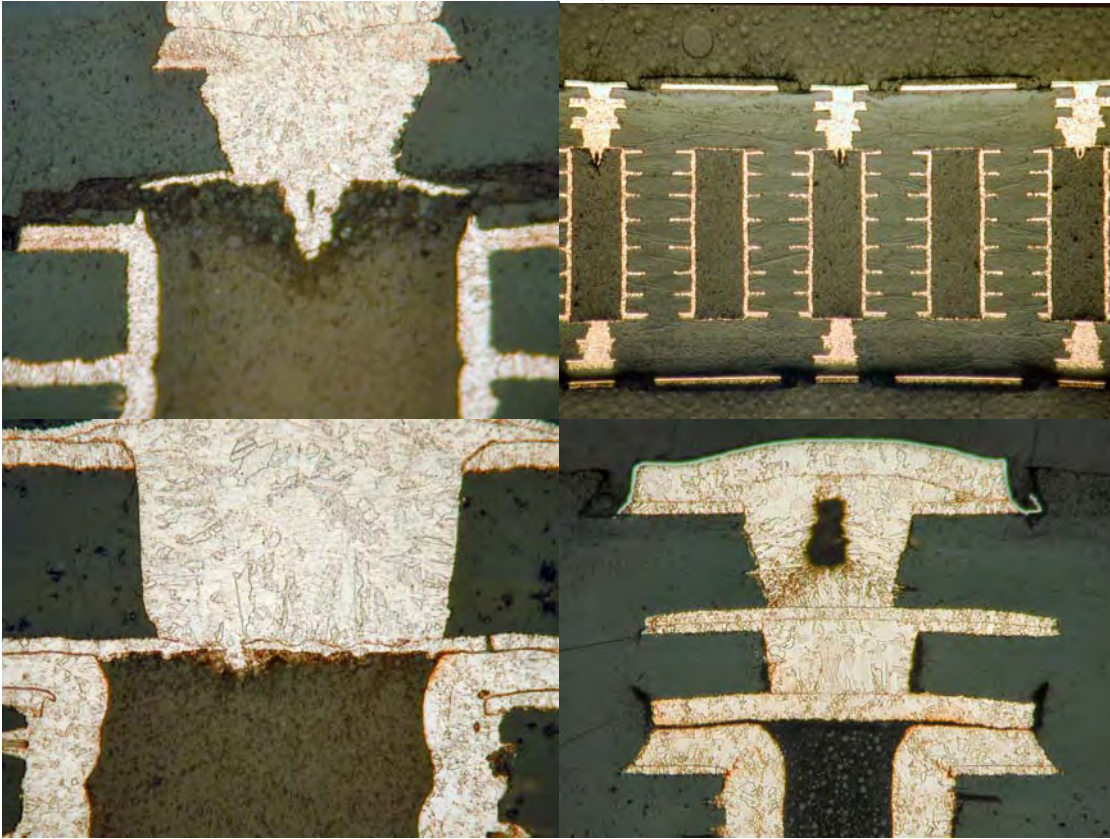


**TARGET PAD CRACKS** – Like knee/corner cracks microvia target pads can cracks, they sometimes referred to as ‘microvia pull out”, they occurs in response to the z-axis expansion or CTE mis-match creating stresses between the capture pad and the target pad. This failure mode is more often observed in thin substrate and flex circuits, especially those with an acrylic adhesive which usually have a higher CTE and lower Tg. If a stacked microvia structure use a non-copper fill material the via is required to have a conductive cap plated. The copper cap creates two secondary concerns; a) low adhesion strength between the electrolytic copper and the fill material, b) the relatively low ductility, elongation, tensile and peel strength of the plated copper compared to traditional copper foil.

Photo 17



Photo's 18, 19, 20 and 21

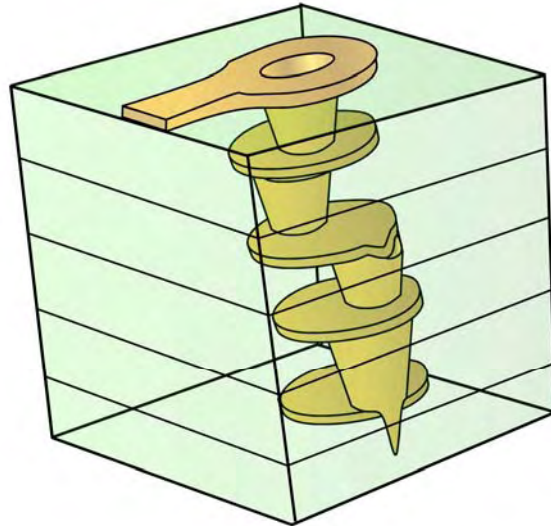


**MICROVIA MIS-REGISTRATION** – There are two types of microvia mis-registration for single level structures; a) ablated hole to the capture pad, b) ablated hole to the target pad. In both cases these condition can result in opens or shorts that are detected by the PWB manufacturers automatic test equipment (ATE). Short circuits can be created in both the x/y and z directions; the z direction is due to the laser ablating through dielectric material adjacent to the edge of the pad, potentially penetrating down to an under-lying feature. The reliability concern would be the compromised/reduced dielectric spacing which would be vulnerable to a conductive anodic filament (CAF) type failure mode. The fact that a microvia is mis-registered does not necessarily signify a reduction in thermal cycles to failure, unless the reduced contact area is combined with a condition where the adhesion to the target pad has been compromised

The combined influence of all manufacturing tolerances must be applied to each sequential lamination cycle, creating diverse registration concerns for stacked micro via structures. Registration systems must accommodate the increasingly challenging influences of tolerances associated to the primary collective effects of inter-layer material movement, laser ablation to feature alignment and direct or photo imaging registration. Each of these critical manufacturing process steps must be tightly controlled to avoid the risk of via to pad breakout, this requirement is further complicated by the multiplication of each individual tolerance level must be factored into a stacked micro via structure.



**Figure 10**



When considering the extreme complexities involved in assuring perfect registration in the build-up of a multi-level micro via structure it becomes statistically inevitable that misalignment will occur at one or more levels. This reality is realized during the micro-section analysis, although quantifying the extent of the condition is very difficult to determine. A traditional vertically ground and polished micro-section is capable of only exposing 1 degree of the via structures circumference, resulting in the remaining 359 degrees not being available to complete visible assessment. Figure 10 illustrates a condition where the surface microvia appears perfectly registered, the three lower levels of interconnection can misalign to the point of via to pad breakout.

**Figure 11**

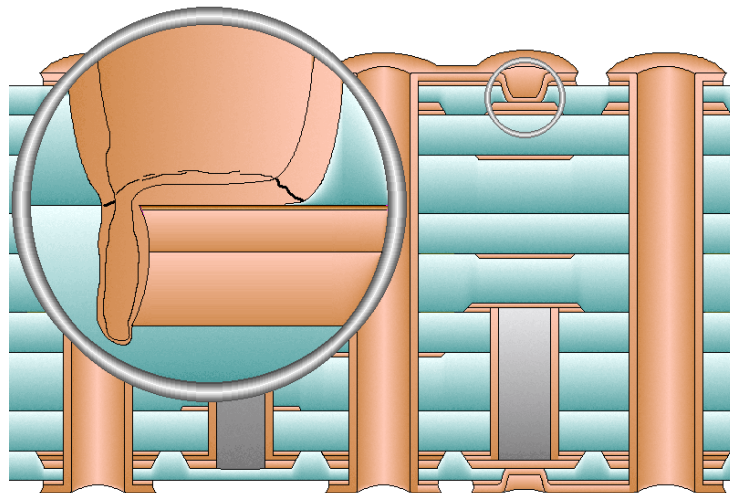




Photo 22

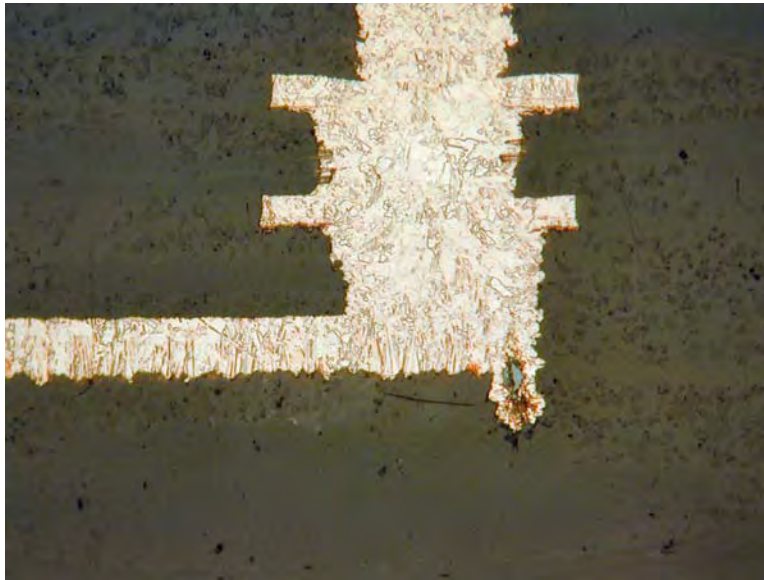
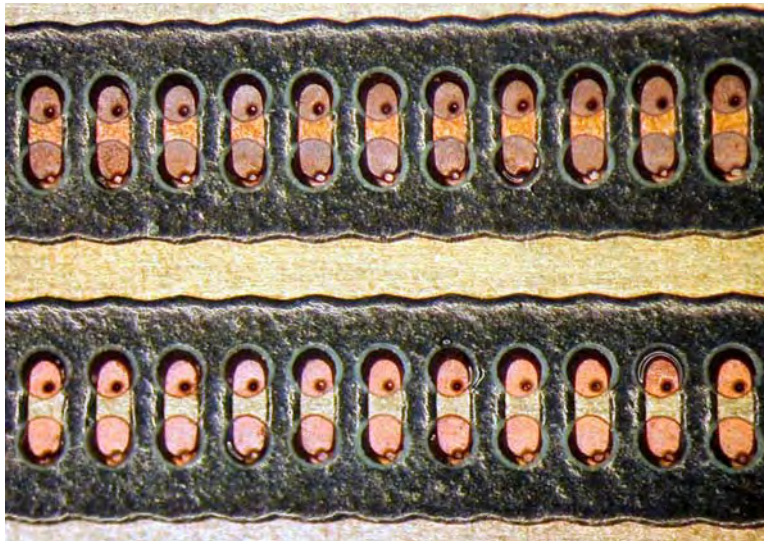
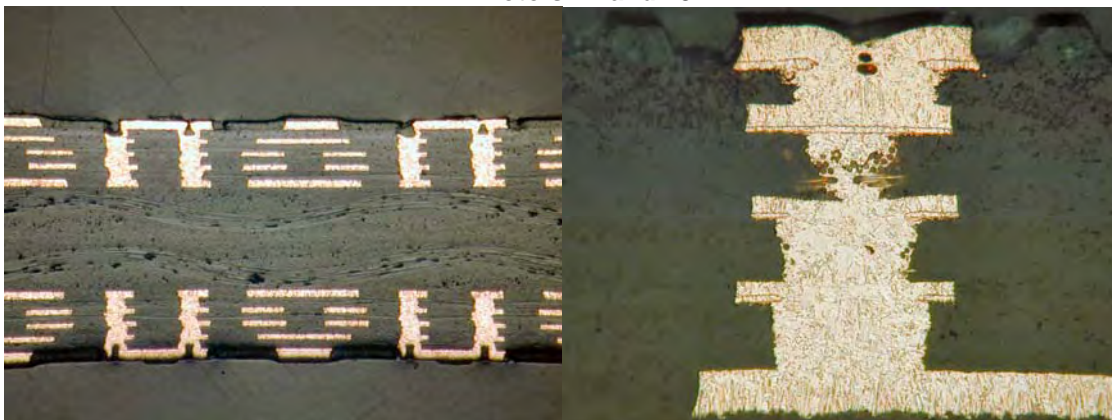


Photo 23



Photo's 24 and 25



**THE PHYSICS OF THE TEST VEHICLE** - The coupon design is the most critical constituent required to establish the ability to successfully detect a failure mode. Most reliability engineers understand the reality that during electrically measurement the sensitivity of the critical areas of interest are small fractions of the test circuit's bulk resistance. This situation is dramatically amplified when testing microvias, due to the smaller geometries involved. The major responsibility of any microvia reliability effort is the ability to create specifically designed test vehicles containing interconnect structures that are sensitive enough to measure low-level increases/changes in resistance.

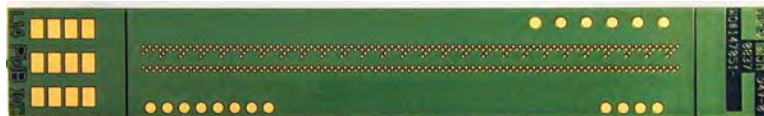
Microvia test circuit designs utilize a combination of mathematical and thermal modeling, in combination with prior experience in the fields of PWB processing, chemistry, materials and statistics. This recipe of skill sets permits a methodology that allows the coupons to be engineered to duplicate the product attributes with the focus on the reliability of the interconnection of interest. The coupon is designed in consultation with the OEM and PWB manufacturer, commonly a negotiation takes place that achieves a location on the production panel large enough to contain hundreds of interconnect structures in order to test a statistically significant sample plan. At no time is the manufacturing process compromised by the introduction of the test coupon, the test vehicle should be "invisible" during the processing of the actual product. The coupons will generally have at least two types of circuits; a powering circuit, used to heat the coupon (and test internal interconnections) and a number of sensing circuits for testing each structure of interest.

**Microvia / Buried Via Coupon  
Photo 24**



For most HDI studies the test vehicle will not contain PTH, this is due to the fact that increasing numbers of products (primarily hand held devices) are designed without through vias. The two or three sense circuits in each coupon design will commonly include structures with the highest combination of vias stacked on top of each other, the smallest ablated diameter, vias ablated onto buried vias, and/or (in simpler product designs) microvias ablated from the outer layers. For statistical purposes and if enough real estate is available/permitted, each test circuit should contain approximately 300 (or more) microvias.

**Microvia Only Coupon  
Photo 25**

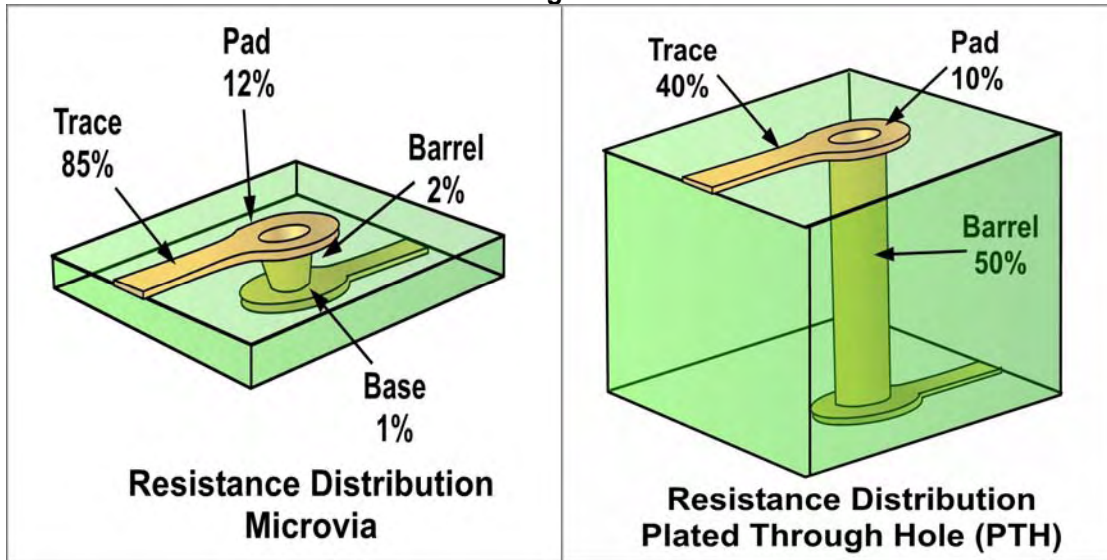


Additional features are designed into the coupons which deliver critical information required to completing both a comprehensive measurement of the product combined with the determination and confirmation of the capability and consistency of the PWB manufacturer. The inclusions are designed to both compliment the reliability coupon by focusing increased attention toward specific material conditions and performance impacts measured before and after exposure to the thermal stresses associated with component assembly and rework.

The reliability portion of the coupon includes the customer's product design rules, which establishes both the products construction and critical attribute sizes, these rules are followed to enable an effective assessment for interconnect reliability. To understand the influence of material change we need to enhance/modify some of these rules to; a) be able to determine important information related to how the product is constructed, b) whether the materials are changing after exposure to the assembly or rework environments, c) where within the construction should problems be expected and d) understanding how the heat is being distributed throughout the product construction.

Each individual area is configured to achieve the highest level of sensitivity for measuring the slight changes that signify material degradation (delamination), moisture removal, Tg, Dk (Dielectric constant), dielectric thickness, temperature distribution (both across the surface and from the surface to the centre of the construction) and fatigue or failure to the interconnect structures. Additional information is available from the author that details each of the sections associated to an HDI coupon design. Refer to Figure 12 for an illustration of how the resistance distribution changes between a microvia and PTH structure, understanding these realities is key to successful coupon design.

Figure 12



The acceptance and rejection standards contain a single criterion for reliability testing, any product under test that exceeds a 10% increase in resistance is deemed failed. Considering a situation where the barrel/via crack was responsible for the coupons failure, using the resistance distribution shown in figure 12 this would require the PTH to effectively increase the bulk resistance by 20% (10% change divided by the barrels ratio of 50%), the microvia would need to increase the bulk resistance by 500% (10% change divided by the barrels ratio of 2%).

To better understand the resistance distribution of various microvia stack configurations see table 1 for a 0.15mm (.006") ablated via and table 2 for a 0.1mm (.004") ablated via. Each table compares the relationship of barrel, trace and pad and identifies the effective of resistance increase required to reach a 10% change. The premise for all product builds was as follows:

- The capture layer started with 17 micron (.00065") copper foil, which was plated to a total thickness of 45 microns (.0018").
- The target pad is 17 micron (.00065") copper foil.
- The capture and target pad diameters are 0.3mm (.012").
- The trace widths are 0.3mm (.012").
- The dielectric distance between the capture(s) and target pad(s) are 0.075mm (.003").
- Total board (10 layer) construction is 1.0mm (.040")
- The microvias are filled with copper

Table 1  
Ablated diameter = 0.15mm (.006")

Microvia Structure	% Via Ratio	% Trace Ratio	% Pad Ratio	Effective Increase
Single	2	86	12	500%
2 Stack	5	84	11	200%
3 Stack	7	82	11	143%
4 Stack	9	80	11	111%
4 + 4 Stack	36	51	13	28%



**Table 2**  
**Ablated diameter = 0.1mm (.004")**

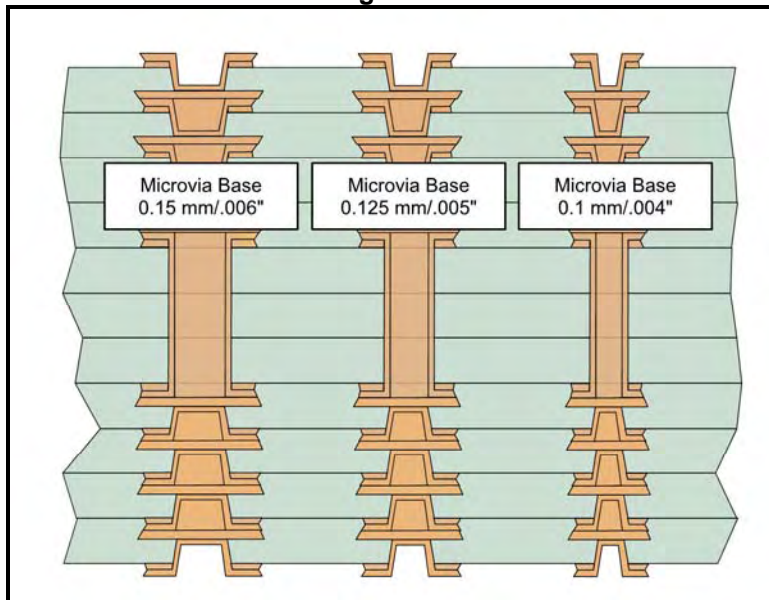
Microvia Structure	% Via Ratio	% Trace Ratio	% Pad Ratio	Effective Increase
Single	4	85	11	250%
2 Stack	9	81	10	111%
3 Stack	13	77	10	77%
4 Stack	17	74	9	59%
4 + 4 Stack	54	38	9	19%

**Note: The 4 + 4 stack is a continuous connection between layer 1 and layer 10 (4 stack on either side of a buried via)**

The influence of the effective resistance increase becomes important only if the failure mode is a wear-out or fatigue driven condition. In situations where the resistance change is immediate (intermittent opens) the small differences in rejection criteria are overwhelmed by the magnitude of change, relative to the bulk resistance.

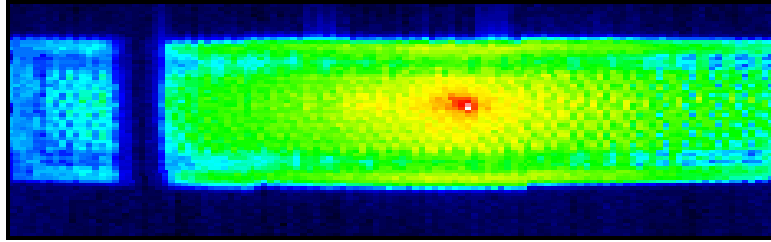
Figure 13 illustrates the relative appearance of 4 + 4 construction with microvia ablated at 3 different diameters.

**Figure 13**

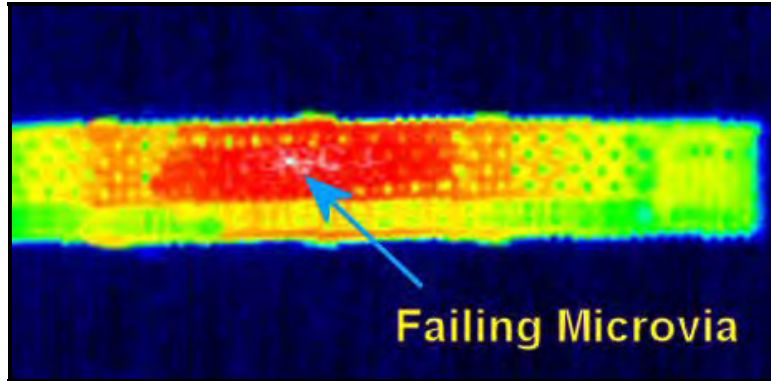


**MICROVIA FAILURE LOCATION** - In an IST evaluation testing automatically stops when a circuit reaches a 10% increase in resistance. The failing coupons have circuits that are still electrically conductive but have a modest increase in resistance. Because the test stopped well before catastrophic failure (open), it is possible to identify the exact microvia that is contributing the highest resistance to the circuit using thermo-graphic techniques. The worst-case microvia, in the coupon, may be identified using thermal imaging cameras in a technique called "failure location". Since the failed circuit has experienced only a 10% increase in resistance, a low level DC current can be applied, permitting the failing interconnection to heat locally. The compromised microvia has a higher resistance, compared to other (robust) microvias, and it will become the hottest structure in the coupon, and easily found using a thermographic camera. The thermographic camera allows direct visualization of the exact location of the weakest microvia (See Photo's 26 and 27). The worst case failing microvia is seen as a high temperature hot spot on the surface of the coupon. This is a powerful tool for finding failure locations for subsequent microsection analysis.

**Thermograph of a Failing Via  
Photo 26**



**Photo 27**



**MICROSECTION PREPARATION** – Microsections were processed as per IPC Test Methods Manual TM 650 2.1.1 Microsection, Manual Method. It should be noted that a mild micro-etch after polishing was applied to allow the improved visualization of microvia structures. Microscopic examinations were conducted up to a maximum magnification of 1250X. Micrographs were digitally captured using a Nikon Cool Pix camera.

**FAILURE ANALYSIS OF MICROVIAS** - The established documented methodology for evaluating microvias by microscopic technique requires that the microvia to target pad be examined without the use of a microetch. Examining an un-etch cross section of a microvia can be used to good effect in fabrication, however, with thermally stressed microvias, that are in the process of failure, it is more effective to use a mild microetch. Typically a mild micro-etch is used to enunciate internal structures within the interconnection. The crystalline structure of the electrolytic copper, the plated layers and thickness' of the electroless copper and micro-inclusions within or between copper layers are easily seen. It also must be noted that an overly aggressive micro-etch can hide subtle internal structures and create artifacts that could be confused with known defects.

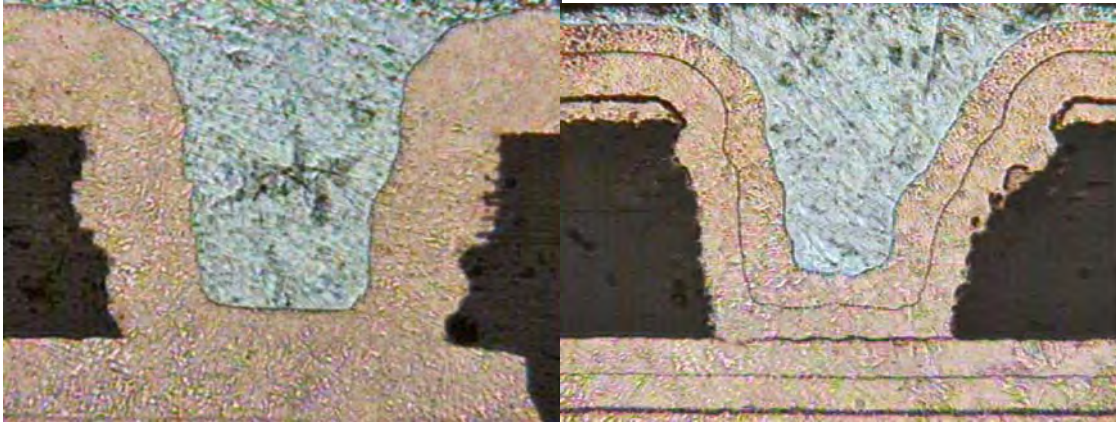
In photos 28 and 29 a good microvia was photographed before and after etching to demonstrate the degree of detail that may be achieved. In photo 29 the layer one foil, electroless copper, interfaces between the bottom of the microvia and the target pad and the plating on the top of the target pad are easily visualized after a microetch. In photo 28 all internal detail is not visible. It was demonstrated that a well-controlled micro etch, using hydrogen peroxide and ammonium hydroxide, greatly enhances the physical details of the failing interconnect and improves the ability to objectively evaluate the causative mechanisms. Armed with these tools a comprehensive failure analysis can be achieved.



## An Un-Etched and Etched Microvia

Photo 28

Photo 29



### Conclusion –

- a) Reliability testing of multi-level microvia structures can be achieved effectively with engineered coupons based on actual product construction design rules.
- b) Accelerated life testing requires test temperatures just above the material Tg to effectively discern product reliability.
- c) Single and 2 stack microvias are generally the most robust type of copper interconnection used in HDI applications, increasing the technology to 3 stack and 4 stack requires concerted effort to assure product reliability.
- d) Ranking the inherent reliability of 3 stack and 4 stack structures to other interconnects like plated through holes, blind, or buried vias, may need to be reconsidered in future reliability test programs.
- e) The advent of lead/free assembly and rework temperatures has increased the stress experienced by the PWB substrate. These higher thermal excursions degrade the reliability of all interconnections and materials. The reliability of microvia structures used for meet the challenges of HDI applications must be assessed following exposure to the lead/free assembly environment.
- f) Thermal cycle testing of microvias is effective at 190°C for FR4 based dielectrics material, these increased temperatures effectively demonstrate that robust structures can survive beyond 3000 thermal cycles.
- g) Changes in failure mode should be expected between single, two, three and four stack microvia structures relative to their relationship to and attachment to internal structures (buried vias) toward the center of the PWB construction.
- h) The failure modes associated with multi-level stacked microvia structures include microvia base to target pad separation, microvia barrel cracks, corner cracks, target pad “pull out”, and failures due to mis-registration.

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### Reference Documents:

Microvia Reliability - Concerns in the Lead Free Assembly Environment – Paul Andrews, Gareth Parry, Paul Reid 2005

The Effect of Functional Pads and Pitch on Via Reliability using Thermal Cycling and Interconnect Stress Testing - Christopher Hunt and Martin Wickham (National Physical Laboratory) Bill Birch and Jason Furlong (PWB) 2009

IPC Test Methods Manual TM650, Method 2.6.26, DC Current Induced Thermal Cycle Test  
IPC Test Methods Manual TM 650 2.1.1 Microsection Method Manual.  
IPC T50 Terms and Definitions

**Bibliography:**

Bill Birch is President of PWB Interconnect Solutions Inc., a supplier of Reliability Test Equipment and Test Services to all segments of the electronics industry. Bill has been involved in the PWB manufacturing industry for over 30 years, he has been responsible for developing the principles of Interconnect Stress Testing (IST) for the past 20 years, receiving multiple patents. He has worked diligently to establish IST technology as the industry standard for the assessment of PWB substrate reliability. IST equipment is now installed at every major PWB manufacturer throughout North America and Asia and is recognized as an effective tool for measuring both process capability and product reliability.